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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,031	CIOACA, DUMITRU	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *2,14,16,18-23,25,27-35,38,40 and 42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13,15,17,24,26,36,37,39,41, and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendment filed on 11 July 2005.

2. Applicant's election without traverse of group I, claims 1 – 13, 15 – 17, 24 – 26, 36 – 37, and 39 – 43 in the reply filed on 11 July 2005 is acknowledged.

3. Claims 14, 18 – 23, 27 – 35, and 38 are withdrawn from consideration.

4. Claims 2, 16, 25, 40, and 42 have been cancelled.

5. Claims 1, 3 – 13, 15, 17, 24, 26, 36 – 37, 39, 41, 43, amended and presented for examination.

6. Examiner thanks applicant for clarifying, and pointing out the limitations of claim 43 in specification with respect to drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 36 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Takahashi et al. [hereinafter as Takahashi], US Patent 6,771,729 B1.

8. As to claim 36, Takahashi discloses a power supply apparatus comprising:

   a. a plurality of charge pump circuits [A, B, fig. 1];

b. a control circuit [UP and DN signal generating circuit] having a data input [Input DATA] and at least one control output [UP, DN], said at least one control output [UP, DN] being operatively connected [as shown in fig. 1] to more than one of said plurality of charge pump circuits [A, B], said control circuit adapted to activate said more than one of said plurality of charge pump circuits in response to a signal on said data input [DATA][col. 3, lines 51 – 67, col. 4, lines 1 – 7, 22 – 45, col. 5, lines 24 – 32, col. 6, 25 – 48, col. 8, lines 18 – 34].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 3 – 13, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi, US Patent 5,193,198, and further in view of Hsu et al. [hereinafter as Hsu], US Patent 6,507, 237 B2.

10. As to claims 1, 15, 24, 39, 41, and 43, Yokouchi teaches an apparatus and method for controlling power supply including central processing unit [26 CPU] receiving and reading input data [through data bus 28], generating a control signal [43] based on information, feeding [receiving through data bus 26] control signal [43] to charge pump enable register [42] with charge pump circuit [44] connected to clock generation circuit [24] and modifying and activating [by enabling charge pump circuit 44] a power to a load in response to control signal [col. 4, lines 57 – 67, col. 5, lines 1 –67, col. 6, lines 1 – 15, fig. 2].

However, Yokouchi does not teach to use a plurality of charge pumps circuits and activating [enabling] more than one of the plurality of charge pump circuits.

Hsu teaches voltage [power] generator with a cascaded charge pumps circuits [200, 210, 220, 230, positive pumps] and activating more than one [210, and 230] of plurality of pumps [200, 210, 220, 230] response to control signal [S2][col. 4, lines 49 – 67, col. 5, lines 1 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 56].

It would have been obvious to one of ordinary skill in art, having the teachings of Yokouchi and Hsu before him at the time of invention was made, to modify the charge pump circuit disclosed by Yokouchi to include a plurality of cascaded charge pumps as taught by Hsu, in order to obtain a substantially smooth output voltage and increases overall pump efficiency by 50% [col. 5, lines 51 - 60].

11. As to claim 3, Hsu teaches enabling more than one of plurality of clock circuits [OSCF1, OSCF2, OSCFS] and driving respective charge pumps [col. 6, lines 61 – 67].

12. As to claim 4, Yokouchi teaches a single-chip microcomputer [10, fig. 2] and RAM [12] including a digital data bus [28] including configuration.

13. As to claim 5, Yokouchi teaches that the control signal is a digital signal [col. 4, lines 62 – 64, fig. 2].

14. As to claim 6, Yokouchi teaches a crystal oscillator [20] to generate oscillation signal to clock generator is an analog signal [col. 4, lines 40 – 67, fig. 2].

15. As to claims 7 – 8, Yokouchi teaches single-chip microcomputer with an external IC [12, RAM] by means data lines and control lines [col. 4, lines 21 – 31, fig. 2] which inherently includes teaching of a voltage signal having proportional to a multiple of data bits of a data word on bus including four data bits having particular state.

16. As to claim 9 – 10, Yokouchi teaches generating voltage signal by flowing an electric current through a voltage divider circuit [col. 8, lines 21 – 38, fig. 9].

17. As to claim 11, Yokouchi teaches that load comprises a digital memory circuit [12, RAM][col. 4, lines 21 – 23, fig. 2].

18. Claims 12 – 13, 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi, US Patent 5,193,198, and further in view of Hsu et al. [hereinafter as Hsu], US Patent 6,507, 237 B2 as applied to claims 1, 3 – 11, above, and further in view of Chevallier et al. [hereinafter as Chevalier], US Patent 5, 313, 429 [cited in previous office action].

19. As to claims 12, and 13, Yokouchi teaches an apparatus and method for controlling power supply including central processing unit [26 CPU] receiving and reading input data [through data bus 28], generating a control signal [43] based on

information, feeding [receiving through data bus 26] control signal [43] to charge pump enable register [42] with charge pump circuit [44] connected to clock generation circuit [24] and modifying and activating [by enabling charge pump circuit 44] a power to a load in response to control signal [col. 4, lines 57 – 67, col. 5, lines 1 –67, col. 6, lines 1 – 15, fig. 2].

However, Yokouchi does not teach to use a plurality of charge pumps circuits and activating [enabling] more than one of the plurality of charge pump circuits.

Hsu teaches voltage [power] generator with a cascaded charge pumps circuits [200, 210, 220, 230, positive pumps] and activating more than one [210, and 230] of plurality of pumps [200, 210, 220, 230] response to control signal [S2][col. 4, lines 49 – 67, col. 5, lines 1 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 56].

However, neither Yokouchi nor Hsu teaches that the memory circuit comprises a flash memory circuit and storing digital data signal as a word in flash memory [programming].

Chevallier teaches charge pump circuit for internally generating a high voltage for programming and erase operations of flash memory and EPROM circuits including based on the decoding command signal triggers the charge pump section to generate high voltage [col. 3, lines 20 – 67, col. 4, lines 1 – 39, fig. 1 – 3].

It would have been obvious to one of ordinary skill in art, having the teachings of Yokouchi, Hsu and Chevallier before him at the time of invention was made, to modify the charge pump circuit disclosed by Yokouchi to include a plurality of cascaded charge pumps as taught by Hsu, and the external memory circuit including a flash memory for

programming and erase operations does not require an external high voltage supply for program and erase operations [col. 6, lines 14 - 19].

20. As to claim 17, Chevallier teaches the subcircuits [102, 112] each include a respective charge pump circuit [300-A,... 300-H] and wherein said activating [enabling] said subcircuits further comprises enabling a clock circuit [250-A,clock control unit] connected to drive said respective [300-A] charge pump circuit [col. 4, lines 9 – 67, col. 5, lines 1 – 67, fig. 3].

21. As to claim 26, Hsu teaches plurality of power supply portions comprises a charge pump circuit [fig. 4].

22. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, US Patent 6,653,888, B2 [cited in previous office action] and further in view of Chevallier et al. [hereinafter as Chevallier], US Patent 5,313, 429 [cited in previous office action].

23. As to claim 37, Lee teaches a power supply apparatus [internal voltage generator] comprising: a plurality of charge [voltage] pump circuits [120_I to 120_n and 140_I to 140-m, fig. 2]; an input bus having a plurality of input lines [input bus having plurality of input lines is inherent to memory]; a control circuit [240, pump control unit] connected to bus and control circuit adapted to provide a particular plurality of output signals [SI , S2,] in response to a number of bits of a predetermined logic value [zero] in an input signal transmitted on said input lines; a plurality of groups of outputs [S1 , S2] of said control circuit [240], each group of outputs [S1, and S2] being operatively connected to a respective charge pump circuit [Vbb pump unit, Vpp pump unit], said outputs being adapted to transmit said plurality of output signals to said plurality of

charge pumps by their respective group and controlling the number of base voltage pumps for generating voltage [col . 2, lines 2 - 30, lines 52 - 67, col . 3, lines 18 - 44, col. 4, lines 27 - 67, fig. 2].

However, Lee does not teach explicitly that plurality of charge pumps are each activated or deactivated in response to said respective plurality of groups of output signals.

Chevallier teaches a memory circuit with charge pump section for internally generating a high voltage for programming and erase operations of flash memory and EPROM circuits including plurality of charge pump circuits [102, low current charge pump, 112, high current charge pump, fig. 2], input having a plurality of inputs lines [fig. 1] and control circuit [10, state control command register] based on decoding (sensing) command signal triggers to enable and disable the respective charge pump section to generate high voltage [col. 3, lines 20 – 67, col. 4, lines 1 – 39, fig. 1 – 3].

It would have been obvious to one of ordinary skill in art, having the teachings of Lee, and Chevallier before him at the time of invention was made, to modify the memory device disclosed by Lee to include a plurality of charge pump circuits, which enables and disables respective charge pump based on the decoding command signal as taught by Chevallier to generate high voltage for programming and erase operations does not require an external high voltage supply for program and erase operations [col. 6, lines 14 - 19].

24. Claims 39, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokouchi, US Patent 5,193,198, and further in view of Chevallier et al. [hereinafter as Chevallier], US Patent 5,313, 429 [cited in previous office action].

25. As to claims 39, 41, and 43, Yokouchi teaches a microprocessor [26, CPU], a data bus [28], and an electronic memory device [12, RAM] connected by means of data lines and control lines and charge pump circuit [44] with charge pump enable register [42] enable signal [44], connected to clock generation circuit [24] and modifying and activating [by enabling charge pump circuit 44] a power to a load in response to control signal [col. 4, lines 57 – 67, col. 5, lines 1 –67, col. 6, lines 1 – 15, fig. 2].

However, Yokouchi does not teach that the memory device [12, RAM] include a power supply and power supply controller having plurality of data bus inputs, a sense circuit adapted to activate or deactivate the output in response to corresponding pattern of data bus signals detected.

Chevallier teaches a memory circuit with charge pump section for internally generating a high voltage for programming and erase operations of flash memory and EPROM circuits including charge pump circuits, and based on the pattern of data bus signals [decoding (sensing) command signal] triggers to enable and disable the charge pump section to generate high voltage [col. 3, lines 20 – 67, col. 4, lines 1 – 39, fig. 1 – 3].

It would have been obvious to one of ordinary skill in art, having the teachings of Yokouchi, and Chevallier before him at the time of invention was made, to modify the memory device disclosed by Yokouchi to include a memory with charge pump circuits,

which enables and disables based on the pattern of data bus signals [decoding command signal] as taught by Chevallier to generate high voltage for programming and erase operations does not require an external high voltage supply for program and erase operations [col. 6, lines 14 - 19].

26. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

27. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Response to Arguments

28. Applicant's arguments with respect to claims 1,15, 24, 36,37, 39, 41, and 43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
July 25, 2005

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